HIGH SPEED ANALOG TO DIGITAL CONVERTER

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of Application No. 10/349,073, Filed: January 23, 2003, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER, which is a Continuation of Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan MULDER; which is a Continuation-in-Part of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER et al.; is a continuation of Application No. 10/158,773, filed on May 31, 2002, Titled: SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING; Application No. 10/158,774, Filed: May 31, 2002; Titled: ANALOG TO DIGITAL CONVERTER WITH INTERPOLATION OF REFERENCE LADDER, Inventors: MULDER et al.; and Application No. 10/158,193, Filed: May 31, 2002, Inventor: Jan MULDER; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan MULDER et al., all of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to analog to digital converters (ADC's), and more particularly, to reducing nonlinearities and inter-symbol interference in high-speed analog to digital converters.

Related Art

[0003] A subranging analog to digital converter (ADC) architecture is suitable for implementing high-performance ADC's (i.e. high speed, low power, low area, high resolution). **FIG. 1** shows a generic two-step subranging architecture, comprising a reference ladder **104**, a coarse ADC **102**, a switching matrix **103**,

a fine ADC **105**, coarse comparators **107**, fine comparators **108** and an encoder **106**. In most cases, a track-and-hold **101** is used in front of the ADC. In this architecture, an input voltage is first quantized by the coarse ADC **102**. The coarse ADC **102** compares the input voltage against all the reference voltages, or against a subset of the reference voltages that is uniformly distributed across the whole range of reference voltages. Based on a coarse quantization, the switching matrix **103** connects the fine ADC **105** to a subset of the reference voltages (called a "subrange") that is centered around the input signal voltage.

[0004] Modern flash, folding and subranging analog to digital converters (ADC's) often use averaging techniques for reducing offset and noise of amplifiers used in the ADC. One aspect of averaging is the topology that is used to accomplish averaging, i.e., which amplifier outputs in which arrays of amplifiers are averaged together.

[0005] In general, flash, folding and subranging ADC's use cascades of distributed amplifiers to amplify the residue signals before they are applied to the comparators. These residue signals are obtained by subtracting different DC reference voltages from an input signal V_{in}. The DC reference voltages are generated by the resistive ladder (reference ladder) **104** biased at a certain DC current.

[0006] High-resolution ADC's often use auto-zero techniques, also called offset compensation techniques, to suppress amplifier offset voltages. In general, autozeroing requires two clock phases (ϕ_1 and ϕ_2). During the auto-zero phase, the amplifier offset is stored on one or more capacitors, and during the amplify phase, the amplifier is used for the actual signal amplification.

[0007] Two different auto-zero techniques can be distinguished, which are illustrated in **FIGs. 2** and **3**. The technique shown in **FIG. 2** connects an amplifier **201** in a unity feedback mode during the auto-zero clock phase ϕ_1. As a result, a large part of the amplifier **201** input offset voltage is stored on input capacitors **C1a, C1b**. The remaining offset is stored on output capacitors **C2a, C2b** if available.

[0008] The second technique, shown in **FIG. 3**, shorts the amplifier **201** inputs during the auto-zero phase ϕ_1 and connects them to a DC bias voltage V_{res}. Here, the amplifier **201** output offset voltage is stored on the output capacitors **C2a**, **C2b**. Many ADC architectures use a cascade of several (auto-zero) amplifiers to amplify the input signal prior to applying to the comparators **107, 108**. In general, flash, folding and subranging ADC's use arrays of cascaded amplifiers, and averaging and interpolation techniques are used to improve performance.

[0009] Unfortunately, the performance of cascaded arrays of amplifiers degrades significantly at high clock and input signal frequencies. The cause of this degradation is illustrated in **FIG. 4** when the reset technique shown in **FIG. 3** is used, and where R_{SW} is shown as a circuit element, and the current flow I_C is explicitly shown.

[0010] When the amplifier **201** is in the auto-zero phase ϕ_1, the input capacitors **C1a, C1b** are charged to the voltage V_{sample} that is provided by the track-and-hold amplifier **101**. As a result, a current I_C will flow through the input capacitors **C1a, C1b** and an input switch (not shown). Due to the finite on-resistance R_{SW} of the input switch (see **FIG. 4**), an input voltage is generated, which will settle exponentially towards zero. This input voltage is amplified by the amplifier **201** and results in an output voltage that also slowly settles towards zero (assuming the amplifier **201** has zero offset).

[0011] Essentially, the auto-zero amplifier **201** is in a "reset" mode one-half the time, and in an "amplify" mode the other one-half the time. When in reset mode, the capacitors **C1a, C1b** are charged to the track-and-hold **101** voltage, and the current I_C flows through the capacitors **C1a, C1b** and the reset switches, so as to charge the capacitors **C1a, C1b**.

[0012] When the ADC has to run at high sampling rates, there is not enough time for the amplifier **201** output voltage to settle completely to zero during the reset phase. As a result, an error voltage is sampled at the output capacitors **C2a, C2b** that is dependent on the voltage V_{sample}. This translates into non-linearity of the ADC, and often causes inter-symbol interference (ISI).

[0013] The problem of ISI occurs in most, if not all, ADC architectures and various approaches exist for attacking the problem. The most straightforward approach is to decrease the settling time constants. However, the resulting increase in power consumption is a major disadvantage.

[0014] Another approach is to increase the time allowed for settling, by using interleaved ADC architectures. However, this increases required layout area. Furthermore, mismatches between the interleaved channels cause spurious tones. The ISI errors can also be decreased by resetting all cascaded amplifiers during the same clock phase. Unfortunately, this is not optimal for high speed operation either.

SUMMARY OF THE INVENTION

[0015] The present invention is directed to an analog to digital converter topology that substantially obviates one or more of the problems and disadvantages of the related art.

[0016] There is provided an analog to digital converter including a reference ladder, a clock having phases ϕ_1 and ϕ_2, and a track-and-hold amplifier tracking an input signal with its output signal during the phase ϕ_1 and holding a sampled value during the phase ϕ_2. A plurality of coarse amplifiers each input a corresponding tap from the reference ladder and the output sign. A plurality of fine amplifiers input corresponding taps from the reference ladder and a signal corresponding to the output signal, the taps selected based on outputs of the coarse amplifiers. A circuit responsive to the clock receives the signal corresponding to the output signal, the circuit substantially passing the signal corresponding to the output signal and the corresponding taps to the fine amplifiers during the phase ϕ_2 and substantially rejecting the signal corresponding to the output signal during the phase ϕ_2. An encoder converts outputs of the coarse and fine amplifiers to an N-bit digital signal representing the input signal.

[0017] In another aspect of the present invention there is provided an analog to digital converter including a reference ladder and a two-phase clock having phases ϕ_1 and ϕ_2. A track-and-hold amplifier tracking an input signal with its output signal during the phase ϕ_1 and holding a sampled value during the phase ϕ_2. A plurality of coarse amplifiers each inputting a signal corresponding to the output signal and a corresponding tap from the reference ladder. A switching circuit that receives the signal corresponding to the output signal and has a differential mode transfer function of approximately 1 on the phase ϕ_2 and approximately 0 on the phase ϕ_1. A plurality of fine amplifiers inputting corresponding taps from the reference ladder and the signal corresponding to the output signal through the switching circuit, the taps selected based on outputs of the coarse amplifiers. An encoder converts outputs of the coarse and fine amplifiers to an N-bit digital signal representing the input signal.

[0018] In another aspect of the present invention there is provided an analog to digital converter including a reference ladder and a multi-phase clock. A track-and-hold amplifier tracking an input signal with its output signal during one phase of the multi-phase clock and holding a sampled value during another phase of the multi- phase clock. A plurality of coarse amplifiers each inputting a signal corresponding to the output signal and a corresponding tap from the reference ladder. Switching means that receives the signal corresponding to the output signal and responsive to the multi-phase clock, the means substantially passing the signal corresponding to the output signal to the fine amplifiers during the one phase and substantially rejecting the signal corresponding to the output signal during the another phase. A plurality of fine amplifiers inputting, through the switching means, corresponding taps from the reference ladder and the output signal, the taps selected based on outputs of the coarse amplifiers. An encoder converts outputs of the coarse and fine amplifiers to an N-bit digital signal representing the input signal.

[0019] An analog to digital converter including a track-and-hold amplifier whose output signal tracks an input signal during one clock phase, and holds a sampled

value during another clock phase. A coarse amplifier inputting the output signal and a coarse tap. A transfer matrix that substantially passes a signal corresponding to the output signal during the one clock phase and substantially blocks the signal corresponding to the output signal during the another clock phase. A fine amplifier inputting a fine tap and the output signal through the transfer matrix, the fine tap selected based on an output of the coarse amplifier. An encoder converts outputs of the coarse and fine amplifiers to an N-bit digital signal representing the input signal.

[0020] An analog to digital converter including a differential coarse amplifier inputting a signal corresponding to an input signal and a coarse tap during one clock phase, and a sampled value during another clock phase. A plurality of cross-coupled transistors that substantially pass the first signal and a fine tap during the one clock phase and substantially block the first signal and the fine tap during the another clock phase, the fine tap selected based on a signal from the differential coarse amplifier. A differential fine amplifier inputting an output of the plurality of cross-coupled transistors. An encoder converts outputs of the coarse and fine amplifiers to an N-bit digital signal representing the input signal.

[0021] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0022] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE FIGURES

[0023] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this

specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0024] **FIG. 1** illustrates a conventional averaging topology.

[0025] **FIGs. 2** and **3** illustrate conventional amplifier topologies with reset switches.

[0026] **FIG. 4** illustrates a conventional amplifier topology and the source of the inter-symbol interference problem.

[0027] **FIG. 5** illustrates a source of inter-symbol interference in greater detail.

[0028] **FIG. 6** illustrates one embodiment of the present invention.

[0029] **FIG. 7** illustrates another embodiment of the present invention.

[0030] **FIG. 8** illustrates a reduction in inter-symbol interference using the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0032] Recently, a technique to address the nonlinearity was published by Miyazaki et al., "A 16 mW 30 M Sample/s pipelined A/D converter using a pseudo- differential architecture," ISSCC Digest of Tech. Papers, pp. 174-175 (2002), see particularly FIG. 10.5.2 therein. The technique applies only to amplifiers that use the auto-zero technique of **FIG. 2**.

[0033] In Miyazaki, four extra switches and two extra capacitors are required. The resulting circuit topology has a common-mode transfer function of "1" and a differential-mode transfer function of "0" during the reset clock phase.

[0034] However, an important disadvantage of the circuit shown in Miyazaki is that it requires twice the amount of capacitance. This has a serious impact on the ADC layout area. Furthermore, the capacitive loading of the track-and-hold **101** doubles, which significantly slows down the charging of the capacitors **C1a, C1b** (roughly by a factor of two).

[0035] **FIG. 5** shows the rationale for the present invention. In **FIG. 5**, the track-and-hold amplifier **101** outputs a step function to the sampling capacitors **C1a**, **C1b**. Due to the finite resistance RSW, the pulse becomes a spike (i.e., it is effectively high- pass filtered) by the time it gets to the amplifier **201**, which is the first amplifier in a cascade. The next set of capacitors **C2a**, **C2b** sees a "smeared-out" pulse, which, by the time it is amplified by the next amplifier in a cascade (amplifier **202**), and charges the next stage capacitors **C3a** and **C3b**, becomes further "smeared-out". The spike being transferred throughout the cascaded amplifiers causes inter-symbol interference.

[0036] The problem of ISI can be solved in a very elegant way by complementing the reset switches shown in **FIG. 3** with some additional switches before the fine amplifiers of the fine ADC **105**. The resulting circuit is shown in **FIG. 6**. The extra switches are contained in the dashed box **510** (a transfer matrix or transfer circuit). **FIG. 7** shows a modification of the new circuit that works in a similar way.

[0037] The transfer circuit shown in the dashed box **510** has a transfer function of "1" for common-mode signals at all times, so that the common mode transfer function is HCM (ϕ_1)=1, HCM(ϕ_2)= 1. However, the transfer function varies for differential signals depending on the clock phase (ϕ_1 or ϕ_2). More specifically, the transfer function for differential signals is HDM(ϕ_1) = 0, and HDM(ϕ_2) = 1. Hence, a differential voltage created across nodes ① and ② (due to the charging of the input capacitors **C1a**, **C1b**) is not transferred to input nodes ③ and ④of the amplifier **201** during ϕ_1. Therefore, the output voltage of the amplifier **201** is not affected by $\mathbf{V_{sample}}$ in any way, reducing the occurrence of ISI. The input capacitors **C1a**, **C1b** subtract track-and-hold amplifier **101** voltage from a reference ladder **104** voltage.

[0038] The technique presented herein can find application in various types of ADC architectures that use auto-zero techniques for combating amplifier offsets.

[0039] **FIG. 6** shows one embodiment of the present invention. ϕ_1 and ϕ_2 represent two phases of a clock, preferably non-overlapping phases. As shown

in **FIG. 6**, the sampling voltage V_{sample} is differentially connected to two sampling capacitors **C1a** and **C1b**, which are in turn connected to three switch transistors **Ma**, **Mb** and **Mc**. Gates of the switch transistors **Ma**, **Mb**, **Mc** are connected to ϕ_1, a drain of the transistor **Ma** is connected to V_{res}, and a source of the transistor **Mc** is connected to the reset voltage V_{res}. Between the amplifier **201** and the switch transistors **Ma**, **Mb**, **Mc**, the transfer matrix **510** comprises four transistors **M1**, **M2**, **M3** and **M4**. Gates of the transistors **M2** and **M3** are connected to ϕ_1. Gates of the transistors **M1** and **M4** are connected to V_{dd}, the supply voltage. Sources of the transistors **M1** and **M2** are tied together and to the node ①, which is also connected to the sampling capacitor **C1a**. Sources of the transistors **M3** and **M4** are tied together and also connected to a node ②, which is also connected to the sampling capacitor **C1b**. Drains of the transistors **M3** and **M1** are tied together and to node ③, which is the "+" input of the amplifier **201**. Drains of the transistors **M2** and **M4** are tied together and to node ④, which is also connected to the "-" input of the amplifier **201**.

[0040] Thus, the circuit within the dashed box **510** may be referred to as a transfer matrix that has a property such that its differential mode transfer function $H(\phi_1) = 0$, $H(\phi_2) = 1$. This is different from a conventional approach, where the transfer function may be thought of as being H=1 for both ϕ_1 and ϕ_2.

[0041] It will be appreciated that while the overall transfer function of the transfer matrix **510** is $HDM(\phi_1) = 0$, $HDM(\phi_2) = 1$, $HCM(\phi_1) = 1$, $HCM(\phi_2) = 1$, this is primarily due to the switches **M1**-M4, which essentially pass the differential voltage of nodes ① and ② through to nodes ③ and ④ respectively, on ϕ_2. However, the gain factor need not be exactly 1, but may be some other value. The important thing is that it be substantially 0 on ϕ_1.

[0042] **FIG. 7** represents another embodiment of the present invention. The elements of **FIG. 7** correspond to the same-numbered elements of **FIG. 6**, however, the position of the transfer matrix **510** is before the three transistors **Ma**, **Mb** and **Mc**, rather than after. This results in lower noise operation, compared to the embodiment shown in **FIG. 6**. The embodiment shown in **FIG. 6**,

however, generally allows for higher frequency operation, compared to the embodiment of **FIG. 7**.

[0043] Note that either PMOS or NMOS transistors may be used as switches in the present invention. Note further that given the use of the FET transistors as switches (rather than the amplifiers), the drain and the source function equivalently.

[0044] **FIG. 8** illustrates the improvement in the signal due to the transfer matrix **510**. Note that the transistors **Ma**, **Mb**, **Mc** and the transistors of the transfer matrix **M1**-M4, are PMOS transistors, with the negative supply Vss used instead of the positive supply V_{dd}. As may be seen from **FIG. 8**, the amount of spike seen by the amplifier **201** after a step function outputted from the track-and-hold **101** is dramatically decreased due to the transfer function of the transfer matrix **510**. ϕ_{1e} in **FIG. 8** refers to an "early" phase ϕ_1 of the two-phase clock. The small spike seen in **FIG. 8** is due to a mis-match of the transistors **M1**-M4, and disappears entirely if the transistors are made bigger. In the event there is no spike (i.e., the transistors **M1**-**M4** are perfectly matched), an approximately 50% improvement in speed is expected.

[0045] Note further that in the event of using a plurality of cascaded amplifier stages for a pipeline architecture (designated A, B, C, D), if the A and B stage switches are driven by the phase ϕ_1, and the C and D stages are driven by ϕ_2, the transfer matrix **510** is only needed for the A stage and the C stage. On the other hand, if the switches of the stages A, B, C and D are driven by alternating clock phases (i.e., ϕ_1, ϕ_2, ϕ_1, ϕ_2), each stage will need its own transfer matrix **510**.

[0046] It will be appreciated that the various aspects of the invention as further disclosed in related Application No. 10/158,595, Filed: May 31, 2002, Titled: HIGH SPEED ANALOG TO DIGITAL CONVERTER, Inventor: Jan Mulder; Application No. 10/153,709, Filed: May 24, 2002, Titled: Distributed Averaging Analog To Digital Converter Topology, Inventors: Mulder et al.; Application No. 10/158,773, filed on May 31, 2002, Titled: Subranging Analog To Digital Converter With Multi-Phase Clock Timing; Application No. 10/158,774, Filed:

May 31, 2002; Titled: Analog To Digital Converter With Interpolation of Reference Ladder, Inventors: Mulder et al.; and Application No. 10/158,193, Filed: May 31, 2002, Inventor: Jan Mulder; Titled: CLASS AB DIGITAL TO ANALOG CONVERTER/LINE DRIVER, Inventors: Jan Mulder et al., all of which are incorporated by reference herein, may be combined in various ways, or be integrated into a single integrated circuit or product.

[0047] It will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined in the appended claims. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.